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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,985	01/21/2004	Ming-Cheng Chang	10113681	4317

34283 7590 05/19/2005

QUINTERO LAW OFFICE
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EXAMINER	
TRAN, THIEN F	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 05/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,985	CHANG ET AL.	
	Examiner	Art Unit	
	Thien F. Tran	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *4-7 and 10-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of species 1 represented by Figure 3 with claims 1-3, 8 and 9 readable thereon in the reply filed on 05/03/2005 is acknowledged.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3, 8 and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Clevenger et al. (US 6,399,447).

Clevenger et al. discloses a dynamic random access memory cell layout (Figures 1 and 2), comprising: a first gate conductor pair and a second gate conductor pair extending along a first direction (see Figure 2), in which each gate conductor pair comprises a first gate conductive line 102 and a second gate conductive line 102; a bitline pair extending along a second direction and intersecting the gate conductor pairs, in which the bitline pair comprises a first bitline 101 and a second bitline 101; a first active area extending along the second direction, crossing the first gate conductor pair 102 and corresponding to the first bitline 101; and a second active area extending along the second direction, crossing the second gate conductor pair 103 and corresponding to the second bitline; wherein, each active area comprises: a first deep trench DT and a second deep trench DT formed in a substrate underneath the first gate conductive

line and second gate conductive line 102, respectively; a bitline contact CB (104) formed between the first gate conductive line and the second gate conductive line, in which the bitline contact is electrically connected to the corresponding bitline 101; a common source/drain region 112 formed in the substrate between the first gate conductive line and the second gate conductive line, in which the common source/drain region is electrically connected to the bitline contact; a first vertical transistor formed overlying the first deep trench, in which the first vertical transistor comprises a first buried strap out-diffusion region (n+) formed in the substrate adjacent to one sidewall of the first deep trench; and a second vertical transistor formed overlying the second deep trench, in which the second vertical transistor comprises a second buried strap out-diffusion region (n+) formed in the substrate adjacent to one sidewall of the second deep trench.

Regarding claim 2, the first deep trench is partially overlapped with the first vertical transistor, and the sidewall profile of the first deep trench on the overlapping portion is a line shape.

Regarding claim 3, the second deep trench is partially overlapped with the second vertical transistor, and the sidewall profile of the second deep trench on the overlapping portion is a line shape.

Regarding claim 8, the memory cell layout further comprises a first deep trench capacitor formed at the lower portion of the first deep trench.

Regarding claim 9, the memory cell layout further comprises a second deep trench capacitor formed at the lower portion of the second deep trench.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thien F. Tran whose telephone number is (571) 272-1665. The examiner can normally be reached on 8:30AM - 5:00PM Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

tt
May 15, 2005

Thien Tran

THIEN TRAN
PRIMARY EXAMINER